IN THE CLAIMS:

Please cancel claims 1, 6 and 7, without prejudice.

Please amend claims 2-5 and add new claims 8 and 9 as follows:

2. (Amended) The input circuit of Claim 3, wherein the delay means defines the delay time such that an edge of the clock signal, on which the data signal is intended to be latched and which is included within a transition interval of the data signal, is delayed to a point in time after the transition interval of the data signal is over.

3. (Amended) An input circuit comprising:

delay means for defining a delay time for at least one logical state of a data signal and thereby delaying a clock signal for the delay time defined; and

a holding circuit for holding the data signal responsive to the delayed clock signal;

wherein the delay means comprises:

a comparator for comparing the edge of the clock signal, on which the data signal is intended to be latched, to at least one of leading and trailing edges of the data signal; and

a delay circuit for defining the delay time based on a result of comparison performed by the comparator.

4. (Amended) An input circuit comprising:

delay means for defining a delay time for at least one logical state of a data signal and thereby delaying a clock signal for the delay time defined; and

a holding circuit for holding the data signal responsive to the delayed clock signal;

wherein the delay means comprises:

a comparator for comparing the edge of the clock signal, on which the data signal is intended to be latched, to leading and trailing edges of the data signal;

a first delay circuit for defining the delay time for a logically high state of the data signal based on a result of comparison, performed by the comparator, between one of the leading edges of the data signal and the edge of the clock signal;

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a second delay circuit for defining the delay time for a logically low state of the data signal based on a result of comparison, performed by the comparator, between one of the trailing edges of the data signal and the edge of the clock signal; and

a selector for selecting the delay time defined by the first delay circuit when the data signal is in the logically high state or the delay time defined by the second delay circuit when the data signal is in the logically low state.

5. (Amended) The input circuit of Claim 3, wherein the delay circuit defines the delay time based on the result of comparison performed by the comparator and a setup time for correctly latching the data signal.